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| 10/792,094 | 03/04/2004 | Takao Saotome | HITA.0521 | 4103 |

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|---|---|
| DICKEY, THOMAS L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/792,094 | SAOTOME ET AL. | |
| | Examiner | Art Unit | |
| | Thomas L. Dickey | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *11-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/177,044.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

# DETAILED ACTION

**1.** The preliminary amendment filed on 3/4/2004 has been entered.

### *Oath/Declaration*

**2.** The oath/declaration filed on 3/4/2004 is acceptable.

### *Drawings*

**3.** The formal drawings filed on 03/4/2004 are acceptable.

### *Priority*

**4.** Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/177,044, filed on 6/24/2002.

### *Information Disclosure Statement*

**5.** The Information Disclosure Statement filed on 3/4/2004 has been considered.

### *Claim Rejections - 35 USC § 112*

**6.** The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 11-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**A.** The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

**B.** In the recitals of claims 11-13, 17, 22, and 25 there are 39 separate instances where an element has been referred to without supplying an antecedent basis for the referred-to element. For simplicity, claims 11-13, 17, 22, and 25 are quoted below. Each instance of a lack of antecedent basis is annotated.

> 11. A semiconductor integrated circuit device, comprising a RAM macro, including: a first region, a second region and a third region which are respectively formed in the **[lacking antecedent]** square shape and are disposed continuously in this sequence in the **[lacking antecedent]** first direction; a fourth region, a fifth region and a sixth region which are respectively formed in the **[lacking antecedent]** square shape and are disposed continuously in this sequence in said **[lacking antecedent]** first direction; and a seventh region, an eighth region and a ninth region which are respectively formed in the **[lacking antecedent]** square shape and are disposed continuously in this sequence in said **[lacking antecedent]** first direction, wherein said first, fourth and seventh regions are continuously disposed in this sequence in the **[lacking antecedent]** second direction which is perpendicular to said **[lacking antecedent]** first direction, wherein said second, fifth and eighth regions are continuously disposed in this sequence in said **[lacking antecedent]** second direction, wherein said third, sixth and ninth regions are continuously disposed in this sequence in said **[lacking antecedent]** second direction, wherein a first memory array including a plurality of first memory cells is formed to said first region, wherein a second memory array including a plurality of second memory cells is formed to said third region, wherein a third memory array including a plurality of third memory cells is formed to said seventh region, wherein a fourth memory array including a plurality of fourth memory cells is formed to said ninth region, and wherein an input terminal of said RAM macro is disposed to at least one region among said fourth, fifth and sixth regions.
>
> 12. A semiconductor integrated circuit device according to claim 11, wherein said input terminal of RAM macro is connected to a signal line formed on the **[lacking antecedent]** predetermined wiring layer and is extended for disposition from an external side of said RAM macro, and wherein said signal line is not defined with said RAM macro.
>
> 13. A semiconductor integrated circuit device according to claim 11, wherein said signal line is defined with an automatic disposition wiring in the **[lacking antecedent]** chip side.

16. A semiconductor integrated circuit device according to claim 15, wherein said fifth region is disposed to the center of said RAM macro.

17. A semiconductor integrated circuit device, including: a first region, a second region and a third region which are respectively formed in the **[lacking antecedent]** square shape and continuously disposed in the **[lacking antecedent]** first direction; a fourth region, a fifth region and a six region which are respectively formed in the **[lacking antecedent]** square shape and continuously disposed in said **[lacking antecedent]** first direction; and a seventh region, an eighth region and a ninth region which are respectively formed in the **[lacking antecedent]** square shape and continuously disposed in said **[lacking antecedent]** first direction; wherein said first, fourth and seventh regions are continuously disposed in this sequence in the **[lacking antecedent]** second direction which is perpendicular to said **[lacking antecedent]** first direction, wherein said second, fifth and eighth regions are disposed continuously in this sequence in said **[lacking antecedent]** second direction, wherein said third, sixth **["sixth region" lacks antecedent]** and ninth regions are disposed continuously in this sequence in said **[lacking antecedent]** second direction, wherein a first memory array including a plurality of first memory cells is formed in said first region, wherein a second memory array including a plurality of second memory cells is formed in said third region, wherein a third memory array including a plurality of third memory cells is formed in said seventh region, wherein a fourth memory array including a plurality of fourth memory cells is formed in said ninth region, wherein each of said second, fourth, fifth, sixth **["sixth region" lacks antecedent]** and eighth regions is smaller than each of said first, third, seventh and ninth regions, and wherein at least a part of the **[lacking antecedent]** address input circuit is formed in said fifth region.

22. A semiconductor integrated circuit device, including: a first region, a second region and a third region which are formed in the **[lacking antecedent]** square shape and disposed continuously in the **[lacking antecedent]** first direction; a fourth region, a fifth region and a sixth region which are formed in the **[lacking antecedent]** square shape and disposed continuously in said **[lacking antecedent]** first direction; and a seventh region, an eighth region and a ninth region which are formed in the **[lacking antecedent]** square shape and disposed continuously in said **[lacking antecedent]** first direction, wherein said first, fourth and seventh regions are continuously disposed in this sequence in the **[lacking antecedent]** second direction which is perpendicular to said **[lacking antecedent]** first direction, wherein said second, fifth and eighth regions are continuously disposed in this sequence in said **[lacking antecedent]** second direction, wherein said third, sixth and ninth regions are continuously disposed in this sequence in said **[lacking antecedent]** second direction, wherein a first memory array including a plurality of first memory cells is formed in said first region, wherein a second memory array including a plurality of second memory cells is formed in said third region, wherein a third memory array including a plurality of third memory cells is formed in said seventh region, wherein a fourth memory array including a plurality of fourth memory cells is formed in said ninth region, wherein each of said second, fourth, fifth, sixth and eighth regions is smaller than each of said first, third, seventh and ninth regions, and wherein at least a part of the **[lacking antecedent]** clock input circuit is formed in said fifth region.

25. A semiconductor integrated circuit device according to claim 22, wherein the **[lacking antecedent]** tenth region, which is in contact with said first, second, and third regions is further included and the **[lacking antecedent]** data output circuit is formed in said tenth region.

27. (New) A semiconductor integrated circuit device according to claim 12, wherein said signal line is defined with an automatic disposition wiring in the **[lacking antecedent]** chip side.

**C.** Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999).

The term "continuously disposed in said ['first' or 'second'] direction" used *passim* in claims 11,17, and 22, is used by the claim to mean "sequentially aligned", in a particular direction, while the accepted meaning is, essentially, gibberish (An English speaker, even one having skill in the relevant art, is required to guess at the meaning using hints garnered from the drawings and specification). The term is indefinite because the specification does not clearly redefine the term.

The term "formed in the square shape" used passim in claims 11,17, and 22, is used by the claim to mean "formed within the outlines of a square, along with other elements recited as lying within said outlines", while the accepted meaning is, essentially, gibberish (Once again, an English speaker, even one having skill in the relevant art, is required to guess at the meaning using hints garnered from the drawings and specification). The term is indefinite because the specification does not clearly redefine the term.

Correction is required.

## *Claim Rejections - 35 USC § 102*

**7.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**A.** Claims 11-21 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by YAMAGATA ET AL. (6,310,815).

With regard to claims 11-13 and 27 Yamagata et al. discloses a semiconductor integrated circuit device, comprising a RAM macro 3 in the rough shape of a square, including a fifth (37c) region formed in the center of the square; four memory arrays each including a plurality of memory cells and each formed in one of four "corner" regions formed in the corners of said square, said four "corner" regions being known as the first (4ra), third (4sa), seventh (4ta), and ninth (4ua) regions; four "side" regions being known as the second (37a), fourth (4td), sixth (4ud), and eighth (37b) regions; said second (37a) region aligned in a first direction with said first (4ra) and third (4sa) regions and aligned in a second direction with said fifth (37c) region; said second direction being perpendicular to said first direction; said eighth (37b) region aligned in said first direction with said seventh (4ta) and ninth (4ua) regions and aligned in said

second direction with said fifth (37c) region; said fourth (4td) region aligned in said second direction with said first (4ra) and seventh (4ta) regions and aligned in said first direction with said fifth (37c) region; said sixth (4ud) region aligned in said second direction with said third (4sa) and ninth (4ua) regions and aligned in said first direction with said fifth (37c) region; an input terminal 44v of said RAM macro 3, that is disposed to at least one region among said fourth (4td), fifth (37c) and sixth (4ud) regions and connected to a signal line (5e or 5f) formed in a predetermined wiring layer (disclosed, note column 8 lines 28-67, as being either the second aluminum interconnect layer 2A1 or the third aluminum interconnect layer 3A1 of the cross-sectional view shown in figures 2A and 2B) and is extended for disposition from an external side of said RAM macro 3, and wherein said signal line (5e or 5f) is not defined (i.e., does not cross over RAM regions 4ra through 4ua) with said RAM macro 3. Note figures 2A-B, 16, column 8 lines 27-68, column 19 lines 36-59, and column 20 lines 9-25 of Yamagata et al.

The applicant's claims 13 and 27 do not distinguish over the Yamagata et al. reference regardless of the process used to form the signal line ("automatic disposition wiring" means, according to applicant's specification, that the upper layer wiring has been laid using an "automatic disposing and wiring method." Application at paragraph 22. In this examiner's opinion, applicant has failed to enable said "automatic disposing and wiring method." However, because in a product claim such as claim 13 or 27 we consider only the patentability of the device per se, and not the patentability of a method which may be used to make the device, enablement or non-enablement of any

particular method of making the device is a moot question here), because only the final product is relevant, not the recited process of laying said signal line using an automatic disposing and wiring method.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

With regard to claims 14-16 Yamagata et al. discloses a semiconductor integrated circuit device, comprising a RAM macro 3 in the rough shape of a square, including a fifth (37c) region formed in the center of the square so that said fifth (37c) region is disposed to the center of said RAM macro 3; four memory arrays each including a plurality of memory cells and each formed in one of four "corner" regions formed in the corners of said square, said four "corner" regions being known as the first (4ra), third (4ta), seventh (4sa), and ninth (4ua) regions; four "side" regions each smaller than any of said four "corner" regions, said four "side" regions being known as the second (44v),

fourth (37a), sixth (37b), and eighth (44w) regions; said second (44v) region aligned in a first (4ra) direction with said first (4ra) and third (4ta) regions and aligned in a second direction with said fifth (37c) region; said second direction being perpendicular to said first (4ra) direction; said eighth (44w) region aligned in said first (4ra) direction with said seventh (4sa) and ninth (4ua) regions and aligned in said second direction with said fifth (37c) region; said fourth (37a) region aligned in said second direction with said first (4ra) and seventh (4sa) regions and aligned in said first (4ra) direction with said fifth (37c) region; said sixth (37b) region aligned in said second direction with said third (4ta) and ninth (4ua) regions and aligned in said first (4ra) direction with said fifth (37c) region; a word line driver 4rd disposed in said second (44v) and eighth (44w) regions; and an input terminal (part of BANK A or BANK B controls) of said RAM macro 3, that is disposed to at least one region among said fourth (37a), fifth (37c) and sixth (37b) regions. Note figures 2A-B, 16, column 8 lines 27-68, column 19 lines 36-59, and column 20 lines 9-25 of Yamagata et al.

With regard to claims 17-21 Yamagata et al. discloses a semiconductor integrated circuit device, comprising a RAM macro 3 in the rough shape of a square, including a fifth (37c) region formed in the center of the square; four memory arrays each including a plurality of memory cells and each formed in one of four "corner" regions formed in the corners of said square, said four "corner" regions being known as the first (4ra), third (4ta), seventh (4sa), and ninth (4ua) regions; four "side" regions each smaller than any of said four "corner" regions, said four "side" regions being known as the second (44v),

fourth (37a), sixth (37b), and eighth (44w) regions; said second (44v) region aligned in a first (4ra) direction with said first (4ra) and third (4ta) regions and aligned in a second direction with said fifth (37c) region; said second direction being perpendicular to said first (4ra) direction; said eighth (44w) region aligned in said first (4ra) direction with said seventh (4sa) and ninth (4ua) regions and aligned in said second direction with said fifth (37c) region; said fourth (37a) region aligned in said second direction with said first (4ra) and seventh (4sa) regions and aligned in said first (4ra) direction with said fifth (37c) region; said sixth (37b) region aligned in said second direction with said third (4ta) and ninth (4ua) regions and aligned in said first (4ra) direction with said fifth (37c) region; a word line driver 4rd disposed in said second (44v) and eighth (44w) regions; at least a part of an address input circuit and a clock signal generating circuit formed in said fifth (37c) region; and a tenth (3) region, being an end part of said RAM macro 3, in contact with said first (4ra), second (44v), and third (4ta) regions further included, a data output circuit being formed in said tenth (3) region. Note figures 2A-B, 16, column 8 lines 27-68, column 19 lines 36-59, and column 20 lines 9-25 of Yamagata et al.

**B.** Claims 17-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. (6,614,714).

With regard to claims 17-21 Hsu et al. discloses a RAM macro 10 having a portion in the rough shape of a square, including a fifth 26c4 region formed in the center of the square four memory arrays (25) each including a plurality ($24_1$-$24_n$) of memory cells and each formed in one of four "corner" regions formed in the corners of said square, said

four "corner" regions being known as the first 18(d), third 18(b), seventh 18(c), and ninth 18(a) regions; four "side" regions, each smaller than any of said four "corner" regions; said four "side" regions being known as the second (26 – that part of spine 26 formed below fifth region 26c4), fourth (22l), sixth (22r), and eighth (26' – that part of spine 26 formed above fifth region 26c4) regions; said second (26) region aligned in a first (horizontal) direction with said first 18(d) and third 18(b) regions and aligned in a second (vertical) direction with said fifth 26c4 region; said second (vertical) direction being perpendicular to said first (horizontal) direction; said eighth (26') region aligned in said first (horizontal) direction with said seventh 18(c) and ninth 18(a) regions and aligned in said second (vertical) direction with said fifth 26c4 region; said fourth (22l) region aligned in said second (vertical) direction with said first 18(d) and seventh 18(c) regions and aligned in said first (horizontal) direction with said fifth 26c4 region; said sixth (22r) region aligned in said second (vertical) direction with said third 18(b) and ninth 18(a) regions and aligned in said first (horizontal) direction with said fifth 26c4 region; a word driver (note figure 7) disposed in said second (26) and eighth (26') regions; a tenth region (head region 34), being an end part of said RAM macro 10 in contact with said first 18(d), second (26), and third 18(b) regions is further included and a data output circuit is formed in said tenth region; and an address input circuit (note the detail view of fifth 26c4 region shown in figure 2B) and a clock signal generating circuit (once again, note the detail view of fifth 26c4 region shown in figure 2B) disposed formed in said fifth

26c4 region. Note figures 1, 2A-B, 4A-B, 7, column 1 lines 37-62, column 2 lines 8-26, and column y lines 3-32 of Hsu et al.

With regard to claims 22-26 Hsu et al. discloses a RAM macro 10 having a portion in the rough shape of a square, including a fifth 26c4 region formed in the center of the square four memory arrays (25) each including a plurality ($24_1$-$24_n$) of memory cells and each formed in one of four "corner" regions formed in the corners of said square, said four "corner" regions being known as the first 18(d), third 18(b), seventh 18(c), and ninth 18(a) regions; four "side" regions, each smaller than any of said four "corner" regions; said four "side" regions being known as the second (26 – that part of spine 26 formed below fifth region 26c4), fourth (22l), sixth (22r), and eighth (26' – that part of spine 26 formed above fifth region 26c4) regions; said second (26) region aligned in a first (horizontal) direction with said first 18(d) and third 18(b) regions and aligned in a second (vertical) direction with said fifth 26c4 region; said second (vertical) direction being perpendicular to said first (horizontal) direction; said eighth (26') region aligned in said first (horizontal) direction with said seventh 18(c) and ninth 18(a) regions and aligned in said second (vertical) direction with said fifth 26c4 region; said fourth (22l) region aligned in said second (vertical) direction with said first 18(d) and seventh 18(c) regions and aligned in said first (horizontal) direction with said fifth 26c4 region; said sixth (22r) region aligned in said second (vertical) direction with said third 18(b) and ninth 18(a) regions and aligned in said first (horizontal) direction with said fifth 26c4 region; a word driver (note figure 7) disposed in said second (26) and eighth (26') regions; a tenth

region (head region 34), being an end part of said RAM macro 10 in contact with said first 18(d), second (26), and third 18(b) regions is further included and a data output circuit is formed in said tenth region; and at least a part of a clock input circuit (note the detail view of fifth 26c4 region shown in figure 2B) and a clock enable signal input circuit (once again, note the detail view of fifth 26c4 region shown in figure 2B) disposed in said fifth 26c4 region. Note figures 1, 2A-B, 4A-B, 7, column 1 lines 37-62, column 2 lines 8-26, and column y lines 3-32 of Hsu et al.

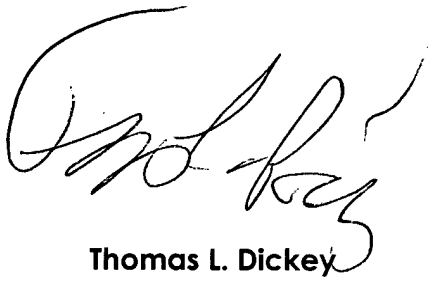
***Conclusion***

**8.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**Thomas L. Dickey**
**Patent Examiner**
**Art Unit 2826**
**10/05**